AMENDMENTS TO THE SPECIFICATION

Please amend the title on the title page and on page 1 as follows:

~~HIGH SPEED MULTIPLIER~~ FILTERING VARIABLE OFFSET AMPLIFIER

Please add the following new paragraph after the title of the application on the first page:

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of U.S. Patent Application Serial No. 10/041,677, which was filed on Jan. 7, 2002, and which issued on Sep. 23, 2003 as U.S. Patent No. 6,624,688, the entirety of which is incorporated herein by reference.

In the specification:

Please replace paragraph 0022 with the following amended paragraph:

--[0022] The second stage 236 includes variable current generator 206, which provides a tail current to transistor pair 218, 220, and a complementary current generator 208, which provides a tail current to transistor pair 222, 224. When the current of generator[[is]] 206 is increased by ΔI, the current of generator 208 is decreased by ΔI, and visa versa. The aggregate current generated by second-stage generators 206 and 208 is twice that generated by first stage generators 202 and 204 in the first stage 234. The inputs to the gates of transistors 218 and 222 is V_{n-1}^{+} and the inputs to the gates of transistors 220 and 224 is V_{n-1}^{-}. The widths of the gates of transistors 220 and 222 are increased (or decreased) by a factor α--

Please replace paragraph 0026 with the following amended paragraph:

--[0026] Consider the first stage 234 in an operating condition wherein $V_n^{+} = V[[_i]]_n^{-}$. Also assume that the tail currents 202 and 204 are equal and the load impedances are equal. In such a configuration, the stage 234 provides a nominal offset that will appear at the output as $V_{out}^{+} - V_{out}^{-} = V_{nominal}$

~~= {[α/(α+1)]I + [1/(α+1)I} R_{load}~~

= {[α/(α+1)]I + [1/(α+1)I} Rload

~~{[α/(α+1)]I + [1/(α+1)I} R_{load} (1)~~

- {[α/(α+1)]I + [1/(α+1)]I} Rload (1)

= 0.

Next, keeping the input voltages the same, if current 202 is increased and current 204 is decreased both by the same amount, namely $I_{202} + \Delta I$ and $I_{204} - \Delta I$, then V_{out}^+ changes to the following:

$$V_{out}^+ = \{[\alpha/(\alpha+1)]\ [I_{202} + \Delta I] + [1/(\alpha+1)][I_{204} - \Delta I]\}\ R_L \qquad (2)$$

Similarly, the new value of V_{out}^- is given by:

$$V_{out}^- = \{[\alpha/(\alpha+1)]\ [I_{204} - \Delta I] + [1/(\alpha+1)]\ [I_{202} + \Delta I]\}\ R_L \qquad (3)$$

Finally, the difference voltage $V_{out}^+ - V_{out}^-$ is given by:

$$V_{out}^+ - V_{out}^- = + [2(\alpha-1)/(\alpha+1)]\ \Delta I\ R_{load} \qquad (4)$$--

Please replace paragraph 0030 with the following amended paragraph:

--[0030] FIG. 3 shows a three-stage filter circuit 300 that is similar to circuit 200 except that an additional stage 346 is added to include the differential signal V_{n+1} in the filtration process. The first stage 348 includes variable current generator 314, which provides a tail current to transistor pair 322, 324, and a complementary current generator 316, which provides a tail current to transistor pair 326, 328. When the current of generator [[is]]314 is increased by ΔI, the current of generator 316 is decreased by ΔI, and visa versa. The inputs to the gates of transistors 322 and 326 is V_n^+ and the inputs to the gates of transistors 324 and 328 is V_n^-. The widths of the gates of transistors 324 and 326 are increased (or decreased) by a factor α.

Please replace paragraph 0031 with the following amended paragraph:

--[0031] The second stage 350 includes variable current generator 318, which provides a tail current to transistor pair 330, 332, and a complementary current generator 320, which

provides a tail current to transistor pair 334, 336. When the current of generator [[is]]318 is increased by ΔI, the current of generator 320 is decreased by ΔI, and visa versa. The average current generated by second-stage generators 318 and 320 is twice that generated by first stage generators 314 and 316 in the first stage 348[[340]]. The inputs to the gates of transistors 330 and 334 is V_{n-1}^{+} and the inputs to the gates of transistors 332 and 336 is V_{n-1}^{-}. The widths of the gates of transistors 332 and 334 are increased (or decreased) by a factor α--

Please replace paragraph 0032 with the following amended paragraph:

--[0032] The third stage 346 includes variable current generator 302, which provides a tail current to transistor pair 306, 308, and a complementary current generator 304, which provides a tail current to transistor pair 310, 312. When the current of generator [[is]]302 is increased by ΔI, the current of generator 304 is decreased by ΔI, and visa versa. The average current generated by third-stage generators 302 and 304 is half that generated by first stage generators 314 and 316 in the first stage 348[[340]]. The inputs to the gates of transistors 306 and 310 is V_{n+1}^{+} and the inputs to the gates of transistors 308 and 312 is V_{n+1}^{-}. The widths of the gates of transistors 308 and 310 are increased (or decreased) by a factor α--

Please replace paragraph 0036 with the following amended paragraph:

--[0036] The circuit of FIG. 4 reflects another modification to the filter circuit of FIG. 1. Filter circuit 400 operates similarly to circuit 100 except that the tail current of second stage 422[[418]] is controlled by varying the widths of the channels of the second stage transistors instead of varying an independent current source.--

Please replace paragraph 0038 with the following amended paragraph:

--[0038] In operation, the first and second stages 420 and 422 function similarly to the first and second stages of the filter circuit of FIG. 1. Namely, the fact that the aggregate tail current set by the width of second-stage transistors 408, 410 is twice that set by the width of first-stage transistors 404, 406 dictates that inputs V_{n-1}^{+} and V_{n-1}^{-} will be amplified twice as much as inputs

V_n^+, V_n^-. The filter circuit 400 thus provides output voltages V_{out}^+ at node 416[[230]] and V_{out}^- at node 418[[232]]. The output voltages will reflect a "weighting" of signals n and n-1 consistent with their relative amplification, just as in the circuit of FIG. 1.--

Please replace paragraph 0039 with the following amended paragraph:

--[0039] The circuit of FIG. 5 reflects a modified version of the circuit of FIG. 4 that permits variable offset control. The circuit of FIG. 5 is comprised of two sub-circuits 530, 532 having the same basic topology as circuit 400 inter-coupled to one another in the same fashion discussed above. The only difference between each of the sub-circuits 530, 532 and the circuit 400 is that widths of the certain of the differential transistor pairs are adjusted by factor α. The currents fed into the sub-circuits 530, 532 are complimentary in the sense that, when the current of generator 512 is increased by ΔI, the current of generator 502 is decreased by ΔI, and visa versa. The remaining aspects of components 502-528 are similar to the parallel components 402-418[[414]] already described above in connection with FIG. 4.--